IMPACT: International Journal of Research in Engineering and Technology
ISSN (P): 2347–4599; ISSN (E): 2321–8843
Vol. 11, Issue 9, Sep 2023, 27–32

MONOPOLAR HYBRID CASCADED DC/DC CONVERTER FOR HVDC POWER SYSTEMS

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Received: 15 Sep 2023 **Accepted: 15 Sep 2023** **Published: 27 Sep 2023**

ABSTRACT

Due to significant advantages such long-distance power transmission, decreased losses, asynchronous grid connections, controllability, system availability, and restricted short-circuit currents, high voltage direct current (HVDC) technology is a crucial part of power systems. Huge amounts of power can be efficiently and cheaply sent across great distances with low loss using HVDC transmission. While balancing the grid, it can also connect asynchronous alternate current (AC) networks. One of the most crucial parts of HVDC power transmission and the foundation of HVDC grid interconnections are DC/DC converters. For medium/high-voltage DC grid connections, DC/DC MMC is a well respected converter architecture. Modern HVDC networks have variable voltage levels, and DC/DC MMC topologies are crucial to these networks. Current systems have high power losses, voltage ripples, and current fluctuations.

KEYWORDS: *Cascaded Converter, HCDC, MMC, Single Switch*

INTRODUCTION

Modular multilevel converters (MMC) are a key advancement in power electronics that have greatly aided the development of high-voltage direct current (HVdc) transmission technology based on voltage source converters (VSC). Numerous MMC-HVdc projects with various voltage ratings have been built around the world in the last ten years. Multiterminal and meshed HVdc grids have drawn a lot of interest from academia and business because of their flexibility and reliability. One of the most important components of upcoming HVdc grids will be a dc/dc converter for matching various voltage ratings.

Using medium-frequency (several hundred Hz) transformer or trapezoidal-waveform transformer can help shrink the size and weight of the ac transformer but this is at the expense of much more difficult insulation and cooling design on account of the induced eddy-current losses in magnetic core as well as the windings. In conclusion, the FTF-MMCs are better suited for converting between high-voltage and medium-voltage systems that have a high dc voltage ratio rather than HVdc connectors with identical voltage ratings [10]. Nonisolated topologies are more desirable for low (1 ratio 1.5) and medium (1.5 ratio 5) voltage ratio connections. Modular multilevel dc/dc converter (MMdc) topologies [18]–[24] have been proposed as an alternative to FTF-MMCs that contain more than one conversion stage and do not require an ac link transformer. As seen in Fig. 1(b), a portion of its SMs can be used by both the high-voltage (HV) and low-voltage (LV) dc sides, allowing for a reduction in the number of semiconductors. However, ac voltages and currents must be introduced in order to keep the power balance of the SM capacitors. In order to filter the injected ac voltages, a sizable reactor is needed at the dc output due to the substantial current stress and power losses. Additional SM strings have been used in [23] and [24] to actively reduce the signal in order to avoid activating the reactor. The autotransformer principle-based dc/dc converter (ATdc), as illustrated in Fig. 1(c), is another nonisolated topology. It consists of two MMCs connected in series on the dc ports, and a partial-power ac transformer is used to connect the ac ports [25]. The rating of the ac transformer and power losses can be decreased since some power can be delivered directly through the dc channel. Additionally, a multiport topology can be easily added to ATdc. The ac transformer in the ATdc, however, needs to be built to endure high dc offset voltage stress across the windings, which will result in a significant cost and size increase in comparison to a normal transformer with an identical power rating.The topology of a new monopolar symmetrical hybrid cascaded dc/dc converter is presented in this work.

Power electronic converters are used in DC systems to convert AC sources to DC and distribute the energy via DC lines. With significant motor-controlled loads and delicate electronic loads, DC distribution becomes desirable for an industrial park. These power electronic converters' quick response times enable both efficient noise filtering and the provision of a highly dependable power supply. Two major issues that prevent DC systems from being as reliable are reduced by the use of power electronic-based converters. Switching between AC/DC/AC and stopping DC current in both normal and fault conditions [16].

EXISTING SYSTEM

In this study, a high-voltage-gain dc-dc converter is presented. The suggested converter has an output side voltage multiplier based on a Dickson charge pump and an input side that resembles a two-phase interleaved boost converter. This converter is more desirable for the integration of renewable sources like solar panels to a 400-V dc bus since it offers continuous input current. The suggested converter can also draw power from two separate sources or from a single source. Additionally, the voltage multiplier employed provides low voltage ratings for capacitors, which could result in size reduction. With supporting simulation findings, a thorough discussion of the converter's design and component selection has been conducted. To validate the analytical findings, a hardware prototype of the suggested converter with Vin=20V and Vout=400V has been created.

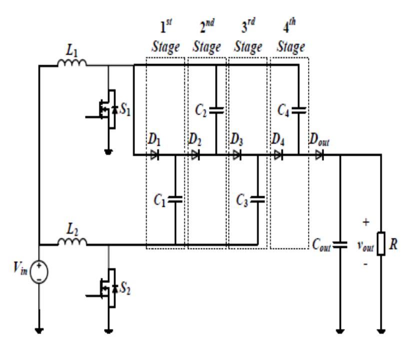

Figure 1: The Circuit of the Single-Stage Resonant Converter.

DRAWBACKS

- High THD due to diode bridge rectifier.
- High power loss.
- Still having voltage and current ripples.

PROPOSED SYSTEM

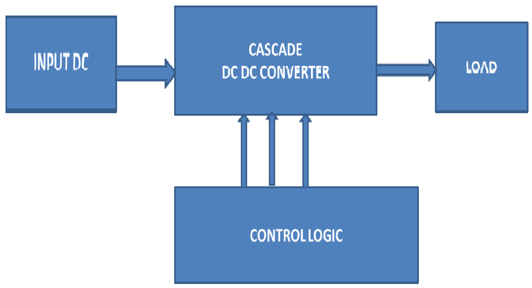

Figure 2: Proposed Block Diagram.

The basic component of the proposed system is a boost converter with a single switch. A PI controller regulates the switch frequency and duty cycle. This can be managed to increase the output voltage.

Figure. 2 depicts the circuit layout of the proposed monopolar symmetrical hybrid cascaded dc/dc converter (MS-HCdc). It consists of four phases (j = a, b, c, d); each phase is composedOf four branches of IGBTs in series connection (Sj1, Sj2, Sj3, Sj4), a string of cascaded half-bridge SMs, and one buffering inductor L. UH is the voltage of the HV dc side while UL is the LV dc side voltage. IH and IL are the currents of the HV and LV sides, respectively. iP j is the SM string current, and uP j is the SM stringvoltage.

Operation Principle of one Phase of the MS-HCDC

One phase of the MS-HCdc is depicted in Figure 3 in operation. In phase an, for instance, power is moved from the HV side to the LV side. IGBT branch voltages range from uSa1 to uSa4, while the operating cycle is Th and uL is the voltage across the buffering inductor. As shown in Fig. 3(a), the SM string is inserted as a result between the positive poles of the HV and LV dc sides because Sa1 and Sa3 are in an ON state during [t0, t5] whereas Sa2 and Sa4 are in an OFF state. The string voltage uP an accommodates UH UL and charges the SM capacitors to control the passage of the string current through Sa1 and Sa3. as shown

$$\Delta E_{\text{charge}} = \int_{t_0}^{t_5} u_{Pa} i_{Pa} \mathrm{d}t = \int_{t_0}^{t_4} (U_H - U_L) I_H \mathrm{d}t$$
$$= \frac{1}{2} T_h I_H (U_H - U_L). \quad (1)$$

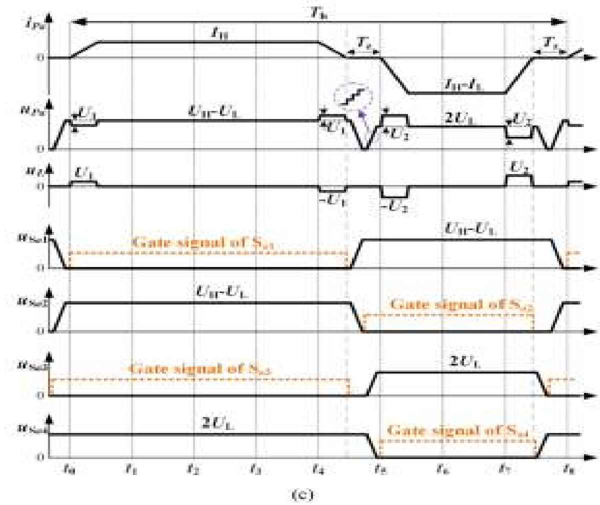

Figure 3:

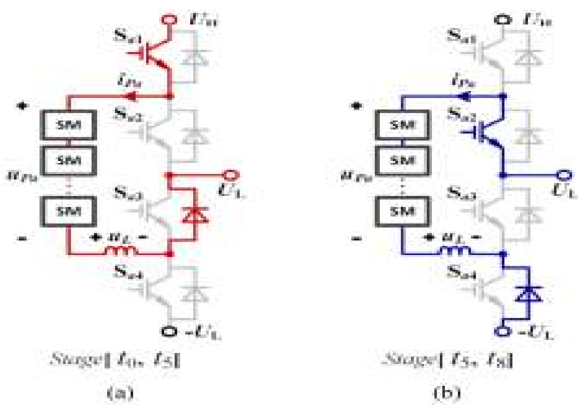

Figure 4:

Figure. Operation principle of phase a of the MS-HCdc. Waveforms (a). (b) Circuit during [t0, t5]. (c) Circuit during [t5, t8]. Sa2 and Sa4 are in the ON state during [t5, t8,] whereas Sa1 and Sa3 are in the OFF state. As seen in Fig. 3(b), the SM string is connected in parallel with the LV dc side. The SM capacitors are discharged when iP a flows through Sa2 and Sa4 and uP an is adjusted to equal 2UL. iP an is controlled as a trapezoid waveform with an amplitude of IHIL, as shown in Fig. 3(c). During an iP falling/rising operation, a negative/positive current driving voltage U2 is imposed across the buffering inductor. The SM capacitors discharge in [t5, t8], and the entire amount of energy released by the SM string is

$$\Delta E_{\mathrm{discharge}} = \int_{t_5}^{t_8} u_{Pa} i_{Pa} \mathrm{d}t = \int_{t_5}^{t_7} 2U_L \left(I_H - I_L\right) \mathrm{d}t$$
$$= \frac{1}{2} T_h U_L \left(I_H - I_L\right). \qquad (2)$$

Thus, when the converter losses are ignored, 2UHIH and 2ULIL stand for the HV-side and LV-side dc power of the MS-HCdc, respectively. Therefore, E is 0, indicating that the energy released and absorbed over one cycle are equal. In actuality, the charging and discharging stages of the string current amplitudes are independently controlled. One amplitude is used to control the converter's power, while the other amplitude is regulated to make sure that the energy absorbed is slightly greater than the energy emitted in order to make up for the converter's power losses. Additionally, an interval Tz is created where iP an is kept at zero during the transition between stages [t0, t5] and [t5, t8]. Sa1 through Sa4 are all switched within Tz as shown in Fig. 3(c), ensuring zero-current switching (ZCS) for the IGBT branches. Additionally, in order to achieve zero-voltage switching (ZVS), the voltages across Sa1-Sa4 (uSa1-uSa4) can be regulated to be zero as well by suitably altering the string voltage uP a. For instance, when Sa1 and Sa3 are turned off, the Sa1 and Sa3, the uP a voltage can be kept at UH − UL, thus uSa1 and uSa3 are maintained zero. On the other hand, before switching ON Sa2, uP a is decreased to zero, as a result, uSa2 becomes zero and ZVS turn-ON of Sa2 is realized. Afterward, uP a is increased to match 2UL, uSa4 drops to zero accordingly and Sa4 also turns ON at ZVS condition.

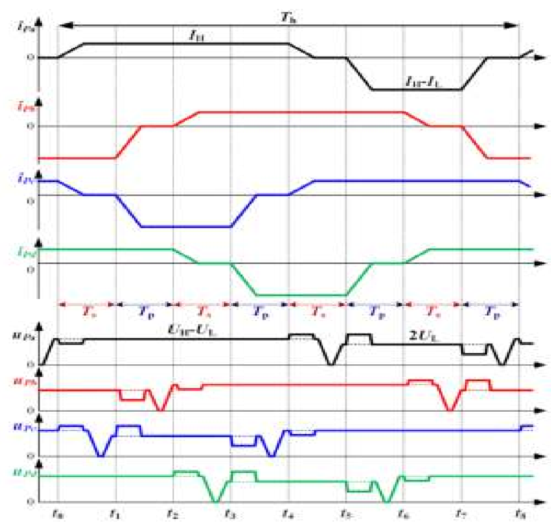

Figure 5: Operation waveforms of the MS-HCDC.

The ZVS situation can likewise be produced by turning ON Sa1 and Sa3 while turning OFF Sa2 and Sa4. As a result, the fluctuation of the string voltage uP an equals UH UL + 2UL = UH + UL during Tz. The length of the string should be chosen to limit dv/dt, or (UH + UL)/Tz. In conclusion, the zero-voltage zero-current switching (ZVZCS) condition allows for the ON and OFF switching of all IGBT branches. Besides, to avoid causing excessive dv/dt in the waveform of uP a, the SMs in the string are switched sequentially, which results in a staircase-shaped transition waveform [17], as shown in Fig. 3(c).

CONCLUSIONS

In this article, an MS-HCdc is suggested for connecting HVdc systems with various voltage ratings. In contrast to the conventional HCdc, the SM strings can be used by both the positive and negative dc poles, necessitating only four phases, which lowers the capital cost, power loss, and converter footprint. When the voltage ratio is more than 2.25, the suggested MS-HCdc has a higher maximum power capacity per semiconductor than the conventional HCdc, hence it should be chosen in this situation to maximize semiconductor use. Discussions are had regarding control methods and operating principles. The MS-HCdc's validity and efficacy were proven by simulation and experimental data. The suggested MS-HCDC may

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